Please delete lines 3-11 on page 16, and replace with the following clean replacement paragraph:

--In addition, the ball contacts 82 are configured for electrical connection to corresponding electrical connectors, such as clips or socket contacts, on the burn-in board 76. The base 80 can be fabricated with conductive vias 58TC, and ball contacts 82 substantially as described in U.S. Patent Application No. 08/726,349, now U.S. Patent No. 5,783,461, entitled "Temporary Semiconductor Package Having Hard Metal, Dense Array Ball Contacts And Method Of Fabrication", which is incorporated herein by reference.--

In the claims

Please cancel claims 40-46.

Please amend claims 25-39 and add claim 47-53. Following is a clean version of the amended and added claims. In addition, a marked version showing the changes to the amended claims follows the Remarks section of this Amendment.

Clean Version Of Amended And Added Claims

25. (amended) A semiconductor component comprising;

a substrate having a first surface and an opposing second surface;

a conductive layer on the first surface;

a plurality of conductors on the first surface defined by a plurality of laser machined grooves through the conductive layer, the conductors comprising portions of the conductive layer electrically isolated from one another by the grooves and separated from one another by remaining portions of the conductive layer;

at least one semiconductor die on the first surface in electrical communication with the conductors;

a plurality of conductive vias in the substrate in electrical communication with the conductors; and

a plurality of external contacts on the second surface in electrical communication with the conductive vias.

26. (amended) The semiconductor component of claim 25 further comprising a plurality of bond pads on the conductors and the semiconductor die is wire bonded to the bond pads.

27. (amended) The semiconductor component of claim 25 further comprising a plurality of bond pads on the conductors and the semiconductor die is flip chip mounted to the bond pads.

28. (amended) The semiconductor component of claim 25 wherein the substrate comprises a material selected from the group consisting of plastic, glass filled resin, silicon and ceramic.

29. (amended) The semiconductor component of claim 25 wherein the external contacts comprise balls in a grid array.

Subt C3

30. (amended) A semiconductor component comprising;

a substrate comprising a surface;

a conductive layer on the surface having a thickness;

a plurality of conductors on the surface defined by a plurality of pairs of laser machined grooves through the thickness of the conductive layer, each conductor comprising a portion of the conductive layer which is electrically isolated on either side by a pair of laser machined grooves; and

a semiconductor die on the surface in electrical communication with the conductors.

31. (amended) The semiconductor component of claim 30 further comprising a laser machined opening in the conductive layer configured for mounting the semiconductor die to the substrate.

cont.

32. (amended) The semiconductor component of claim 30 further comprising a plurality of conductive vias in the substrate in electrical communication with the conductors and with a plurality of contacts on a second surface of the substrate.

33. (amended) The semiconductor component of claim 30 wherein the semiconductor die is flip chip mounted or wire bonded to the conductors.

34. (amended) The semiconductor component of claim 30 further comprising an encapsulant covering the semiconductor die and at least a portion of the surface.

Subt C4

35. (amended) A semiconductor component comprising:

a substrate comprising a surface;

a conductive layer on the surface having a thickness;

a plurality of conductors on the surface comprising portions of the conductive layer, each conductor defined and electrically isolated by a pair of laser machined grooves through the conductive layer; and

a semiconductor die on the substrate in electrical communication with the conductors;

with the thickness of the conductive layer, and a width of the conductors selected to provide a selected impedance for the conductors.

36. (amended) The semiconductor component of claim 35 further comprising an encapsulant covering the semiconductor die and at least a portion of the surface.

cont.

37. (amended) The semiconductor component of claim 35 further comprising a plurality of conductive vias in the substrate in electrical communication with the conductors and with a plurality of external contacts on a second surface of the substrate.

B3

and D5

38. (amended) The semiconductor component of claim 35 wherein the substrate comprises silicon and an electrically insulating layer on the surface.

39. (amended) The semiconductor component of claim 35 wherein the substrate comprises a material selected from the group consisting of plastic, glass filled resin and ceramic.

and C5

47. (added) A semiconductor component comprising;

a substrate comprising a surface;

a conductive layer on the surface; and

B4

a plurality of conductors on the surface defined by a plurality of pairs of laser machined grooves through the conductive layer, the conductors comprising portions of the conductive layer which are electrically insulated from one another by the laser machined grooves, the portions of the

conductive layer including first contacts on first ends thereof configured for bonding, and second contacts on second ends thereof configured for electrical connection to external circuitry; and

a semiconductor die on the substrate bonded to the first pads.

48. (added) The semiconductor component of claim 47 wherein the semiconductor die is flip chip bonded to the first contacts.

49. (added) The semiconductor component of claim 47 wherein the semiconductor die is wire bonded to the first contacts.

50. (added) The semiconductor component of claim 47 wherein the component comprises a chip module, a multi chip module or a package.

51. (added) The semiconductor component of claim 47 wherein the conductive layer comprise a laser machined opening for attaching the die to the substrate.

52. (added) A semiconductor component comprising;

a substrate;

a conductive layer on the substrate;

a plurality of conductors on the substrate defined by a plurality of laser machined grooves through the conductive layer, the conductors comprising portions of the conductive layer electrically isolated from one another by the grooves;

a plurality of contacts on the conductors;

a plurality of conductive vias in the substrate in electrical communication with the conductors; and

a semiconductor die on the substrate in electrical communication with the contacts.

53. (added) The semiconductor component of claim 52 further comprising a plurality of contact balls on the substrate in electrical communication with the conductive vias.